ABSTRACT OF THE DISCLOSURE

A time delay synchronous control scheme for a power supply, which has multiple outputs and tight output regulations, is provided. The switching mode power supply includes (1) a front-end DC/DC converter with current mode output, which can be a LLC Series Resonant converter (SRC) or a flyback converter; (2) one or several post buck converters directly cascaded from the output capacitor of the front-end DC/DC converter; (3) a new scheme of time delay synchronous control used to make the post buck synchronize and modulate from the front-end LLC-SRC or flyback converter. The proposed time delay synchronous control circuit can eliminate the conventional input filter of the post buck converters, as well as reduce the ripple current on the output capacitor of the front-end DC/DC converter, as a result of which, a high efficiency for the overall architecture can be obtained.